

CLAIMS

What is claimed is:

- 5 ~~5/28/17~~
1. A method for etching a feature with minimal RIE lag in an integrated circuit wafer incorporating at least one layer of organosilicate glass dielectric, the method comprising:
- positioning the wafer in a reaction chamber;
- introducing a flow of etchant gas mixture including C₄F₈ and CF₄ into the
- 10 reaction chamber; and
- striking a plasma with the etchant gas in the reaction chamber.
- 11/2/17
- add C₅

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